REMARKS

Summary of Office Action

Claims 1-10 are pending in the above-identified patent application.

Claims 1-10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Owen et al. U.S. Patent No. 4,876,660 (hereinafter "Owen") in view of Simkins et al. U.S. Patent Application Publication No. 2005/0144215 (hereinafter "Simkins").

The rejection of applicants' claims is respectfully traversed.

Applicants' Reply to the § 103 Rejections

The Office Action rejected claims 1-10 as being obvious from Owen and Simkins. This rejection is respectfully traversed.

Applicants claimed invention is generally directed to methods for initializing or zeroing an accumulator value with minimal latency. As recited by applicants' independent claim 1, a first pair of input signals and a second pair of input signals are routed to circuitry that is concentrated in a particular area of a programmable logic resource. For example, the input signals may be routed to one or more multiplier-accumulator blocks. A multiply operation is applied to the second pair of input signals using the circuitry. A feedback output, which is initially set to zero, is applied to the circuitry. The first pair of input signals is

concatenated. The feedback output is concatenated onto the end of the concatenated first pair of input signals. An accumulate operation is then applied to a result of the multiply operation and a result of the concatenating of the feedback output. A result of the accumulate operation is then stored for use as an initialized or zeroed accumulator value.

As recited by applicants' independent claim 8, a pair of input signals is routed to circuitry that is concentrated in a particular area of a programmable logic resource. A multiply operation is applied to the pair of input signals using the circuitry. A register is cleared in the circuitry based on at least one dedicated configuration bit that is set. A feedback output, which is initially set to zero, is applied to the circuitry. The feedback output is concatenated onto the end of the contents of the register. An accumulate operation is then applied to a result of the multiply operation and a result of the concatenating the feedback output. A result of the accumulate operation is then stored for use as an initialized or zeroed accumulator value.

Owen refers to a fixed-point multiplier-accumulator architecture. *See* Owen, Abstract. Owen's FIG. 6A shows a functional block diagram of an emmitter-coupled logic (ECL) multiplier-accumulator. *See* Owen col. 7, 47-61; col. 9, ll. 19-61; and FIG. 6A.

Simkins refers to a field-programmable gate array (FPGA) with a number of cascading digital signal processing (DSP) slices. The DSP slices may be used for multiple mathematical operations. *See* Simkins, Abstract. Simkins'

FIG. 3C shows a schematic of a DSP element or a DSP slice. Simkins' FIG. 14 shows a FPGA having DSP slices. Simkins' FIG. 17 shows a DSP slice that carries out multiply and add operations.

The Examiner alleges that Owen and Simkins show all of the features of the applicant's claimed invention. Applicants respectfully disagree.

Owen and Simkins Do Not Concatenate a Feedback Output Onto the End of the Concatenated First Pair of Input Signals or onto the End of the Contents of a Register

Applicants' independent claims 1 and 8 recite that the feedback output is concatenated onto the end of the concatenated first pair of input signals (independent claim 1) or that the feed back output is concatenated onto the end of the contents of a register (independent claim 8). The Office Action acknowledges that Owen does not disclose concatenating the feedback output onto the end of the concatenated first pair of input signals (Office Action, page 3). The Office Action also acknowledges that Owen does not disclose concatenating the feedback output onto the end of the contents of a register (Office Action, page 5). However, the Office Action contends that Simkins shows both of these features in figures 3C, 14, paragraphs [0121]-[0122] and paragraph [0217], and that it would have been obvious to modify Owen to include these features from Simkins (Office Action, page 3 and page 5). Applicants respectfully disagree and submit that neither Owen nor Simkins, alone or in combination, show applicants' claimed concatenating.

The only concatenating shown in Simkins' figure 3C and discussed in paragraphs [0121]-[0122] is the concatenating of the 18-bit outputs of registers BREG 360 and AREG 362 to form 36-bit output A:B to be sent to multiplier 370. At no point, however, does figure 3C or paragraphs [0121]-[0122] show or suggest concatenating the feedback output (which is initially set to zero) onto the end of the concatenated first pair of input signals as recited by applicants' independent claim 1. Simkins also fails to show or suggest concatenating the feedback output (which is initially set to zero) onto the end of the contents of a register as recited by applicants' independent claim 8. The concatenation of the outputs of two registers is not the same as concatenating a feedback output, which is initially set to zero, onto the end of the concatenated first pair of input signals (independent claim 1) or onto the end of the contents of the register (independent claim 8).

Figure 14 of Simkins also does not show or suggest concatenating the feedback output onto the end of the concatenated first pair of output signals or concatenating the feedback output onto the end of the contents of the register. Rather, figure 14 shows a FPGA having DSP slices. The FPGA has a 36-bit concatenation bus, A:B, on which the high-order 18 bits convey an operand A, and the remaining bits convey an operand B. As such, it is clear that although the concatenation bus may convey 36 bits of concatenated information, this bus, by itself, performs no concatenating as recited by applicants' claims 1 and 8. Additionally, nothing in figure 14 shows

concatenating the feedback output (which is initially set to zero) onto the end of the concatenated first pair of input signals (as defined by applicants' independent claim 1) or onto the end of the contents of the register (as defined by applicants' independent claim 8).

Simkins, paragraph [0217] discusses a 36-bit concatenation of operands, A:B, being input into multiplexing circuitry 1721 shown in figure 17 via an input bus. The input bus can be "sign extended or zero filled as appropriate to 48 bits" (Simkins, paragraph [0217]). The Examiner contends that this shows the step of concatenating as is defined in applicants' claim 1 or claim 8. *See* Office Action, page 3 and page 8. Applicants respectfully submit that sign extending or zero filling a 36 bit input bus to be 48 bits is different than the claimed feature of "concatenating the feedback output onto the end of the concatenated first pair of input signals" as recited by applicants' amended independent claim 1. Sign extending or zero filling a 36 bit input bus to be 48 bits is also different than the claimed feature of "concatenating the feedback output onto the end of the contents of the register" as recited by applicants' amended independent claim 8. Sign-extending or zero-filling a 36-bit number to be 48 bits could produce a result with 12 zero bits at the beginning of the 36-bit number. This is different than concatenating the feedback output (which is initially set to zero) onto the end of the concatenated first pair of input signals (claim 1) or onto the end of the contents of the register (claim 8).

For at least the foregoing reasons, applicants submit that independent claims 1 and 8 are allowable over the prior art of record. Dependent claims 2-7, 9, and 10 are allowable for at least the same reasons. Applicants respectfully request, therefore, that the rejection of claims 1-10 under 35 U.S.C. § 103 be withdrawn.

Conclusion

Applicants respectfully submit that this application, including claims 1-10, is now in condition for allowance. Accordingly, prompt consideration and allowance of this application are respectfully requested.

Respectfully submitted,

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